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TEXAS INSTRUMENTS INCORPORATED
Integrated Circuits Department
Dallas, Texas

HIGH EFFICIENCY TRANSISTOR STRUCTURES

Contract Item No. A2a
Report No. 2

Signal Corps Contract No.
DA 36-039 SC 90806

Department of the Army
Project No. 3A99 21 003

SECOND QUARTERLY PROGRESS REPORT

1 October 1962 to 31 December 1962

US Army Signal Research and Development Laboratory
Fort Monmouth,
New Jersey

HIGH EFFICIENCY TRANSISTOR STRUCTURES

By

Gerald Luecke

Report No. 2

Signal Corps Contract No. DA 36-039 SC 90806

Signal Corps Technical Requirement SCL-7659A
18 December 1961

Department of the Army
Project No. 3A99 21 003

Second Quarterly Progress Report
1 October 1962 to 31 December 1962

Object: To investigate the requirements for the construction of high efficiency micropower silicon transistor structures for general purpose use.

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PURPOSE

The purpose of this program is to design, develop, and fabricate two general purpose, micropower silicon integrated circuits consisting of a digital logic stage and a linear CW amplifier.

These circuits will be constructed by using planar transistor technology and film technology to produce a circuit within and/or on a single chip of silicon.

The final circuits will be enclosed in a hermetic package.

The processes used will be selected to provide the high degree of reliability required by military equipment and shall be applicable to volume production.

The work plan is shown in Figure 1. Circuit design has started, component development continued. Initial layouts for masks to fabricate networks will be processed in the early weeks of the next quarter.

This report still concentrates heavily on component development.

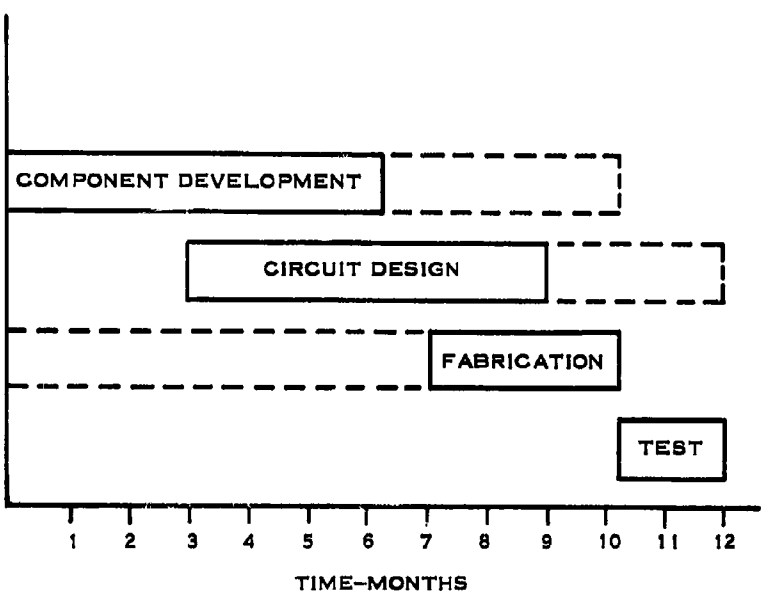


Figure 1. Work Plan

ABSTRACT

Component development continued and circuit development started, especially in the digital area. The linear circuit development is delayed somewhat because the induced-channel field-effect transistor does not have the temperature stability required.

Induced-channel field-effect transistors, lead glass capacitors, and aluminum silicon resistors were fabricated and de-emphasized because of instability and failures in life tests.

Tantalum-Molybdenum resistors were fabricated and will be used in future designs.

Diffused field-effect transistors were fabricated but the I_{DO} was not low enough. Units did not have the back gates isolated.

Circuit design progressed in the digital area to the point of applying components to a specific layout.

Linear circuit design was begun during this quarter.

CONFERENCES

Place: US Army Signal Research and Development Laboratory, Fort Monmouth, New Jersey

Date: 6 November 1962

Attendees:

USASRDL	Texas Instruments
Lt. Jere Hohman	Jack Kilby
Larry Wagner	
Rus Gilsen	

In a conference at USASRDL, the progress on the contract was discussed. The emphasis on field-effect structures was to continue as well as the other component development. Samples of thin-film resistors and capacitors were provided and the data reviewed. Samples of the small-geometry transistors similar to the ones to be used are to be provided as soon as possible.

HIGH EFFICIENCY TRANSISTOR STRUCTURES

Report No. 03-63-

I. COMPONENT DEVELOPMENT

Component development continued on both the induced-channel field-effect transistor and the diffused field-effect transistor. Erratic movement of the I_{DO} curves on the induced-channel field-effect transistor had resulted in a shift of emphasis from this device to the diffused field-effect transistor with very low I_{DO}.

Development of lead-oxide capacitors and silicon-monoxide capacitors continued. The same dielectric effect as observed in induced-channel field-effect transistors seemed to be the cause of failure of lead-oxide capacitors when subjected to life tests.

Development of aluminum-silicon film resistors and refractory metal film resistors of an alloy of tantalum-molybdenum continued with very positive results with tantalum-molybdenum structures.

Transistors with very small geometry - 30 square mil collector areas and 3 square mil emitter areas - were fabricated. Capacitance measurements and characteristic measurements were made on these devices. Initial network layouts will result from these measurements.

II. FIELD-EFFECT TRANSISTORS

A. Induced-Channel Field-Effect Transistors

The process steps for fabricating the induced-channel field-effect transistor were discussed in Quarterly Report No. 1 and the initial channel present at $V_G = 0$ was found to vary with temperature.

The thin dielectric film is a lead glass "grown" by establishing a concentration of lead oxide vapor at the surface of a silicon slice in an oxidizing atmosphere. A source plate is prepared by firing a thin paste of lead oxide and water on a ceramic plate to form a glaze. The glazed plate is suspended above the silicon surface on which the glass is to be formed and the assembly is heated in an air atmosphere.

The thickness of the film is determined by comparing the color of the film with the colors of films of known thickness. Figures 2, 3, and 4 show how the film thickness depends on the time and temperature of heating and the separation of the source-plate and slice. Figure 2 shows an approximate linear growth with time ; Figure 3 shows that the growth rate is roughly inversely proportional to the separation of the source-plate and slice; and Figure 4 shows a proportional relation with temperature.

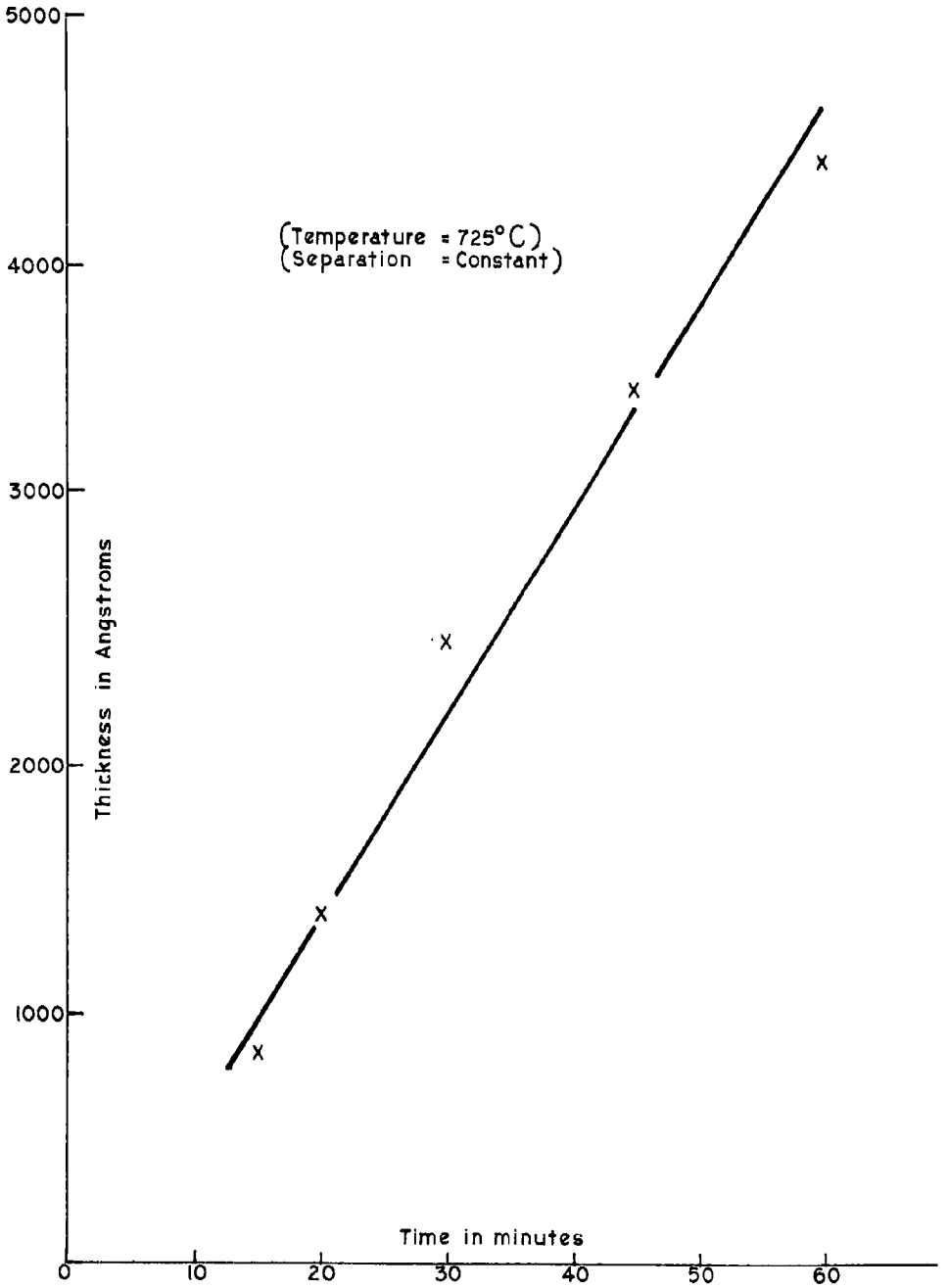


Figure 2. Thickness of Glass Vs Growth Time

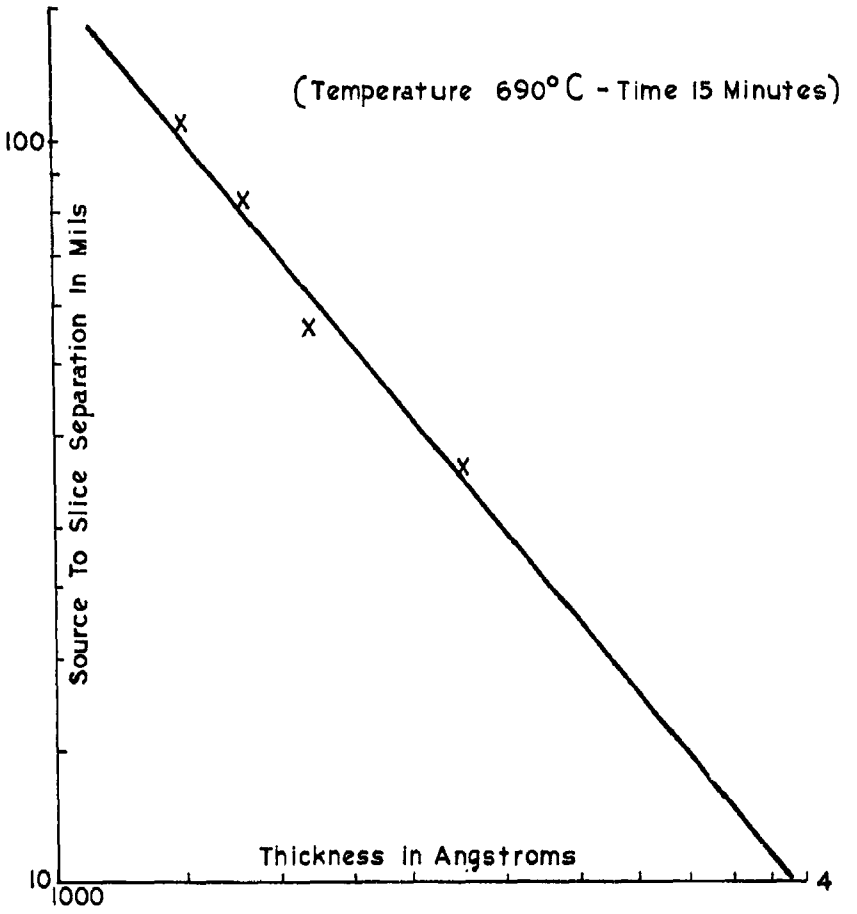


Figure 3. Source to Slice Separation Vs Glass Thickness

Induced-channel field-effect transistor characteristics are shown in Figure 5 and a typical plot of drain current versus gate voltage with constant drain-to-source voltage is shown in Figure 6. Positive voltages on the gate induce an N-type inversion layer in P-type material from N-type source to N-type drain. The variation of drain current with temperature is indicated and this variation caused significant concern.

However, of even more significance was the fact that the drain current varied, dependent upon the gate voltage that was applied at the elevated temperature. Figure 7, curve (a) is the same device as in Figure 6 at 25° C. Curves (b), (c), and (d) show the drain current variation after the device is subjected to 125° C with the various gate voltage applied. Note in particular that curve (d) is a return to initial conditions.

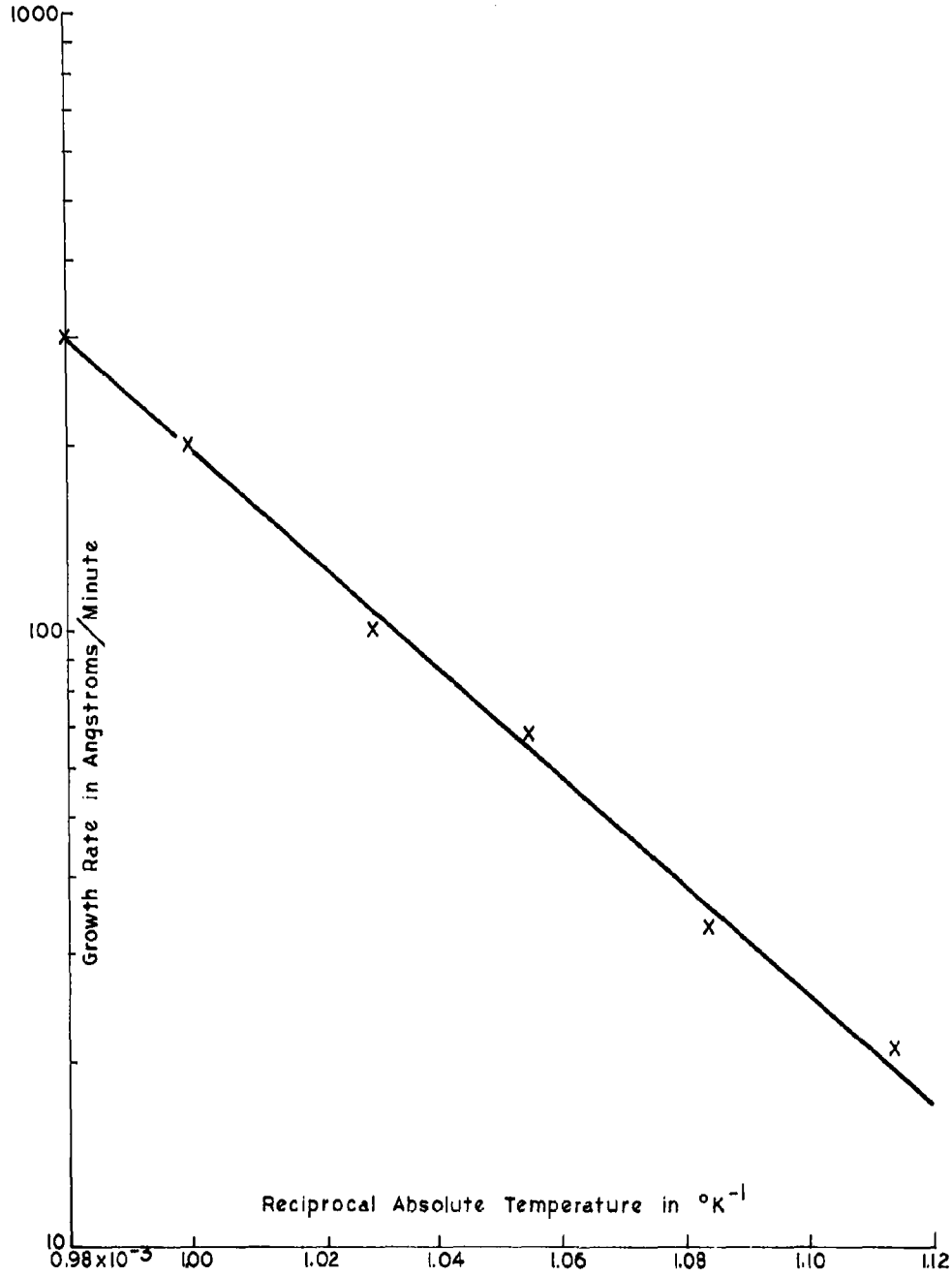


Figure 4. Growth Rate of Glass Vs. 1/K

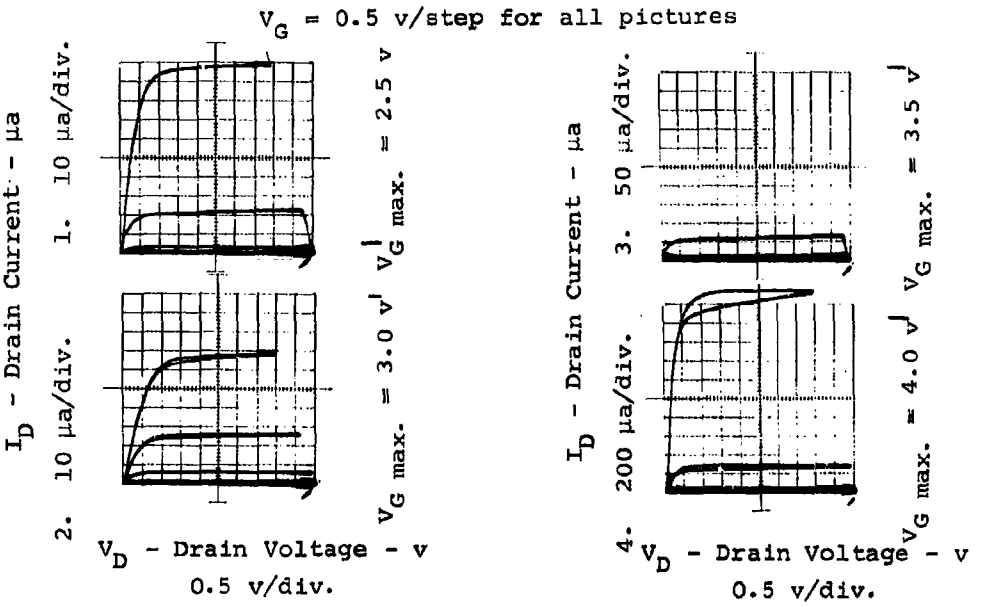


Figure 5. Induced-Channel Field-Effect Transistors

Further expansion of these investigations was carried on by subjecting various devices to extended periods of storage at 125°C. The variations of drain current versus gate voltage characteristics of one such device are shown in Figure 8. Curve (a) is the device before temperature cycling. Curve (f) is the same device after 40 hours of bake. Curve (g) is the device after application of a negative gate voltage instead of positive and shows a drastic change in characteristics (in fact, the negative g_m noted may be turned to good use with future development). After the application of the negative gate voltage, the drain current characteristics have reversed their trend of change with 125°C storage and move in the opposite direction. The original slope is present again.

These phenomena can be explained either by a change in the number of surface states or by a change in the polarization of the dielectric caused by the temperature voltage cycling.

Because of the drastic variation of I_{DO} with temperature, the induced-channel field-effect transistor with the lead glass dielectric seems unsuitable for micropower networks at this time—especially linear where stable bias points are required.

B. Diffused Field-Effect Transistor

Initially, little work was started on diffused field-effect transistor structures because the control problems associated with getting devices

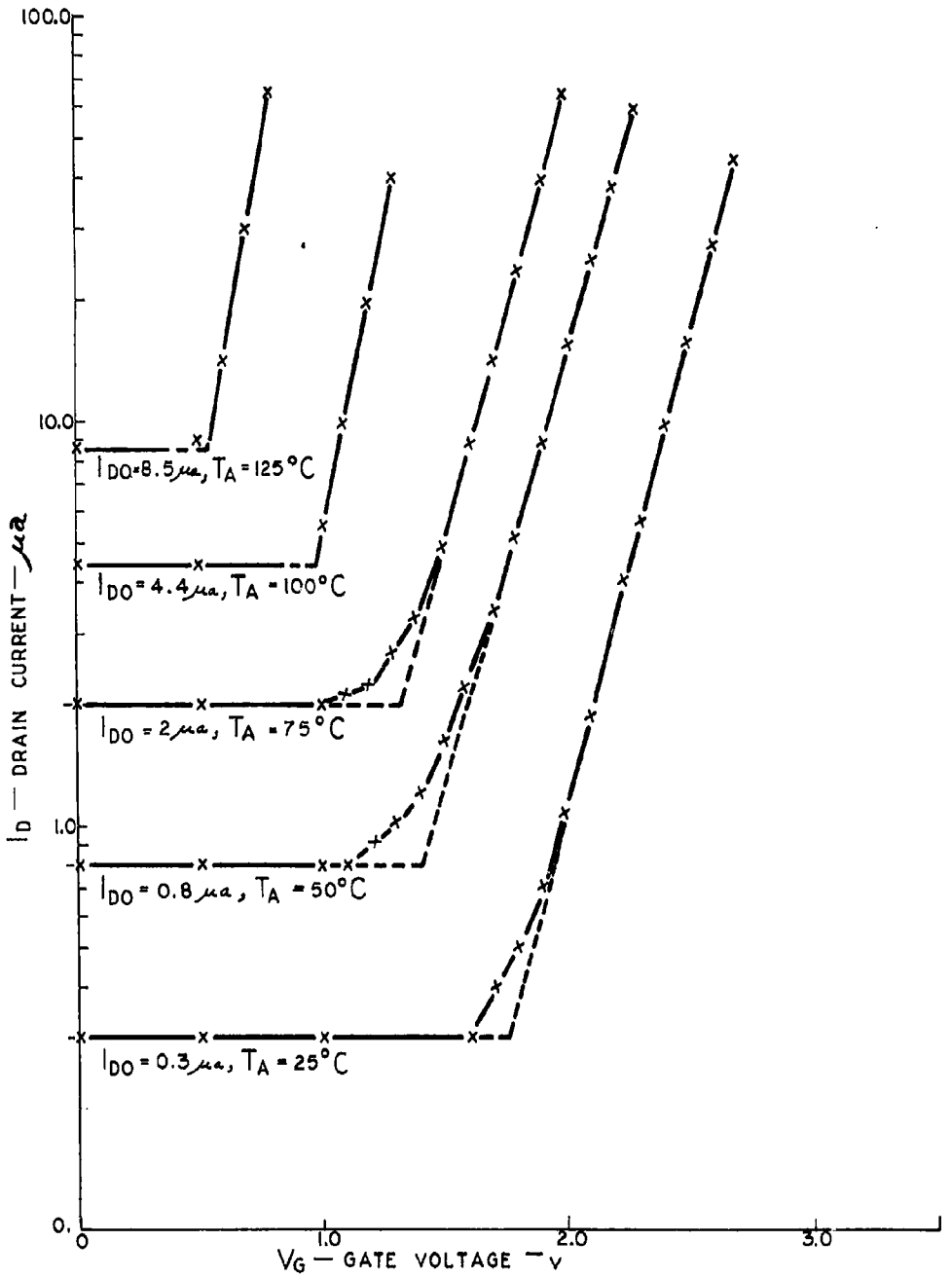


Figure 6. I_D Versus V_G Versus Temperature

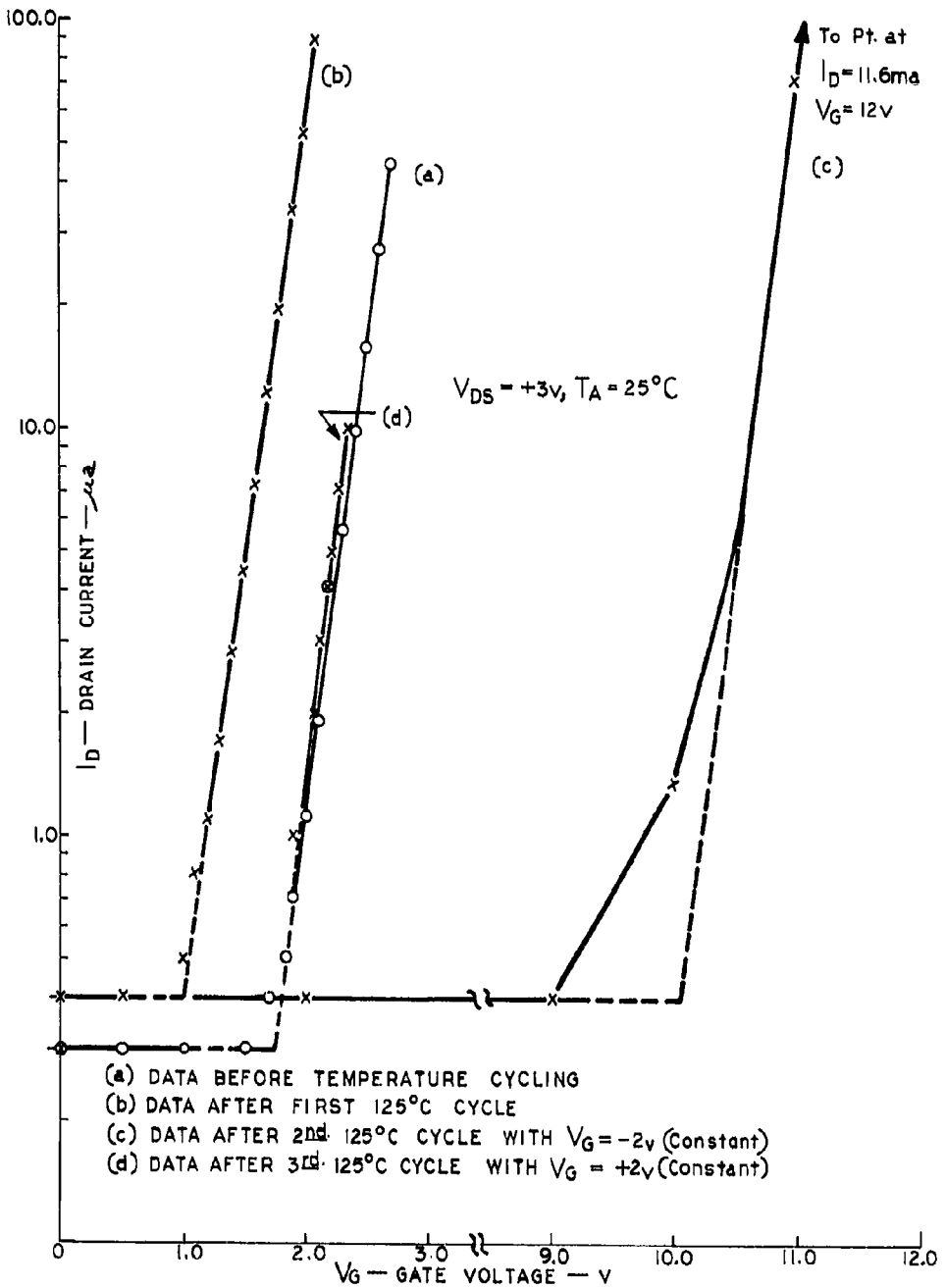


Figure 7. I_D Versus V_G (T cycled)

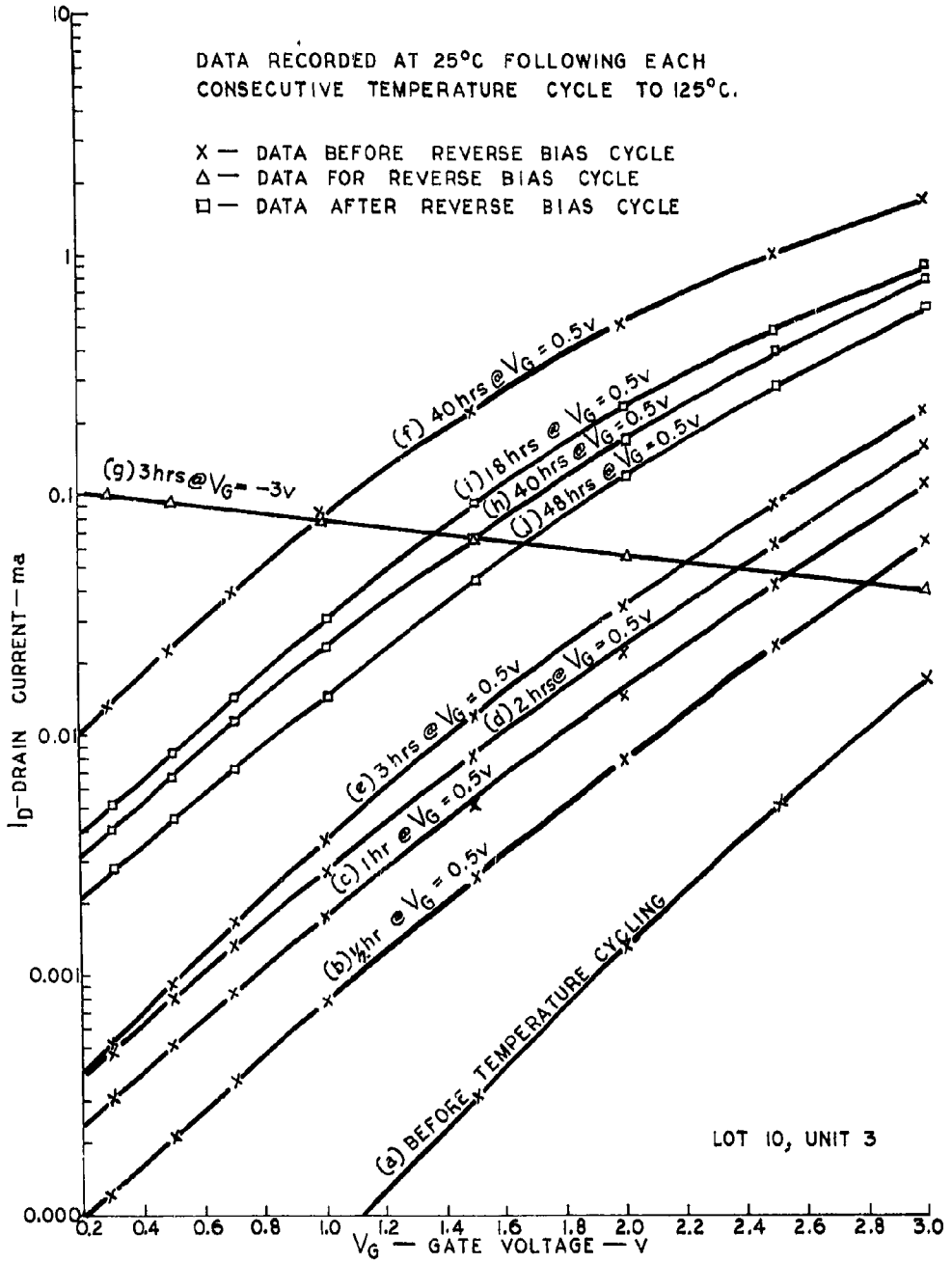


Figure 8. I_D Versus V_G (T cycled with V_G)

consistently at $I_{DO} \leqq 10$ micoramperes seemed much more difficult than the induced-channel field-effect device. However, because of the temperature variations encountered with the induced-channel field-effect transistor, the process control required for the low I_{DO} diffused transistor is being investigated.

Diffused field-effect transistors with characteristics shown in Figure 9 have been fabricated with some success in fully integrated form. However, all back gates of these structures are common. For the CW amplifier circuit, transistors within the network will need their back gates isolated. This presents fairly significant problems because of the low concentration channel diffusion and the narrow channel width. An isolated back gate must have an even lower concentration and must be made on a substrate of a yet lower concentration. Therefore, a more thorough investigation of the basic structure and whether isolation is possible will be initiated.

III. RESISTORS

A. Aluminum-Silicon Dioxide Film Resistors

In Quarterly Report No. 1, the process problems of aluminum silicon dioxide resistors were pointed out. Briefly, the large spread in resistor values and the large negative temperature coefficients were particular problems. The negative temperature coefficients could be overcome by combining with diffused resistors; however, bonding units to tailor the resistor values was necessary.

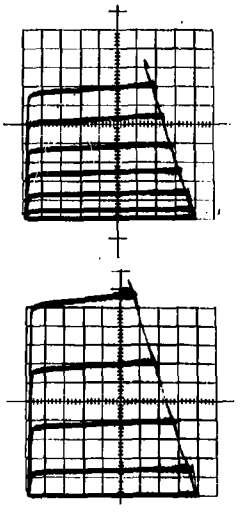


Figure 9. Diffused Field-Effect Transistor Characteristics

Bonding to the aluminum-silicon dioxide has been difficult and requires special processing in a vacuum to provide bonding pads. This step removes the flexibility of bonding anywhere on the resistor.

Because of the lack of adequate process control, the bonding problem and the success of the tantalum-molybdenum resistors, the aluminum-silicon dioxide resistors are not being considered any further at this time. Further development will prove to make this a useful element in the future.

B. Refractory Metal Film Resistors

In Quarterly Report No. 1, the method of evaporation with a non-focused electron beam was discussed. Resistors with 55 ppm/°C were produced with sheet resistivity in the region of 1,000 to 1 megohm per square. It was pointed out that control of resistors above 5,000 ohms per square is quite difficult due to the shape of the curve of evaporation time versus resistance in ohms/square.

Continued work has been in the area of 1,000 to 2,000 ohms per square. Particular problems have been encountered in getting a good reliable contact to the resistors through mounting and bonding. Difficulty has been experienced when aluminum contacts are used; however, successful units have been made using the following process:

Coating the substrate with KMER.

Expose and develop KMER so that a window will be cut through the KMER that is the desired shape for the resistor.

Evaporate a layer of molybdenum and a layer of tantalum for the resistive element.

Remove KMER which removes all molybdenum and tantalum except for the desired resistive element.

Evaporate metal contacts through a metal mask. This area will need considerable investigation since the contact material must not react with or diffuse into the molybdenum tantalum resistor at 450°C, which is mounting temperature. Aluminum has been tried, but reacts. Platinum, silver, gold, and chrome-gold will be investigated.

Heavy investigations will continue in order to make this process compatible with the network processing. These units show good promise.

IV. CAPACITORS

A. Lead-Glass Capacitors

For the micropower circuits, capacitances in excess of one pf/mil^2 are required. These can be realized with thermally grown glass films using a lead glass dielectric, but extremely thin films are required. As reported previously, several lots of these capacitors have been fabricated, some with 1.5 pf/mil^2 and 2.5 volt breakdowns. However, to date, none of an acceptable nature have been able to survive life tests with applied dc voltage.

Seven lots were processed in an effort to optimize film thickness, capacitance per square mil and reliability. These lots were aimed at studying construction variables such as aluminum vs gold contacts, top plates, and back contacts. Of the seven lots, five were scribed, mounted and bonded. Of these five, three lots were put on life tests. These three had back contacts and gold top plates; they were low in capacitance - in the range of 0.2 pf per square mil.

Two of the three lots were step stressed with increasing voltage at intervals of two minutes, ten minutes, and sixty minutes. In each case the voltage was raised ten volts at a time. The results of these last two lots are shown in Figures 10, 11, and 12, where the logarithm of the voltage has been plotted against the total percent which have failed at that point. It appears that a second mode of failure becomes important at around 100 volts in each case. These curves were extrapolated to a 2 percent failure and the points determined by this extrapolation plotted against time in Figure 13. This plot indicates that two percent of the capacitors would fail in 30 minutes with ten volts applied.

It is possible that the mechanisms suggested in the section on induced-channel field-effect transistors for changing the charge distribution in the glass under relatively low voltages might be related to the failure of capacitors using the dielectric under much higher voltages.

Even if these results could be improved, the capacitance per square mil is so low that it is unlikely that reliable devices with the values of capacitance eventually needed for micropower networks will be attained. For this reason, the present glass capacitors are not suitable for micropower network applications.

B. Silicon-Monoxide Capacitors

Few good silicon-monoxide capacitors have been fabricated at this time. The capacitors that have been made have the silicon monoxide dielectric layer between aluminum plates. The capacitors were life tested at 20 v at 125° C and failed between one and two weeks. No attempt was made to passivate these capacitors and the failure mechanism was thought to be slow reaction between the aluminum and silicon monoxide. Difficulties have been experienced in obtaining evaporation masks that will allow depositions at 300° C. Masks made of solid nickel have been obtained and are working satisfactorily.

Two main areas are under investigation to improve the silicon monoxide dielectric characteristics: use of gold for contacts and effect of ultrahigh vacuum on the dielectric.

The investigation of gold contacts includes a different method of depositing the silicon monoxide. This incorporated the use of an evaporation chimney so that the molten silicon monoxide was not in line with the substrate. The chimney stopped any splattering of large particles of silicon monoxide from the source. Units made using the evaporation chimney and gold contacts were subjected to life test at 125° C at 20 v and failed by gradual degradation.

The units evaporated in the 10^{-7} torr range in an ultrahigh vacuum evaporator never exhibited suitable qualities to merit placing them on life test. The reason for failure is not known, unless it can be attributed to the field set up by the ion pumps.

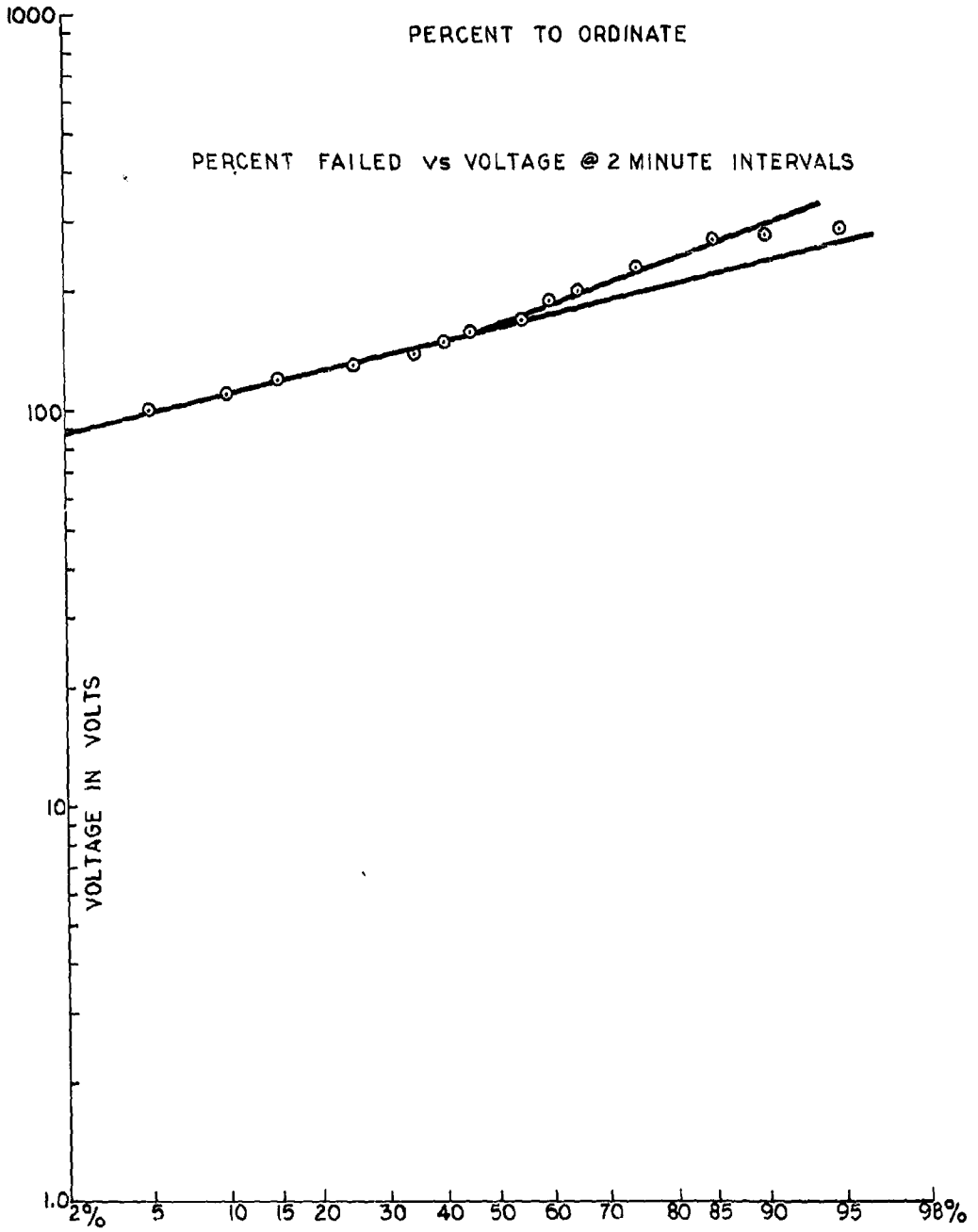


Figure 10. Capacitors Failing at Particular Voltage
2 minute Interval

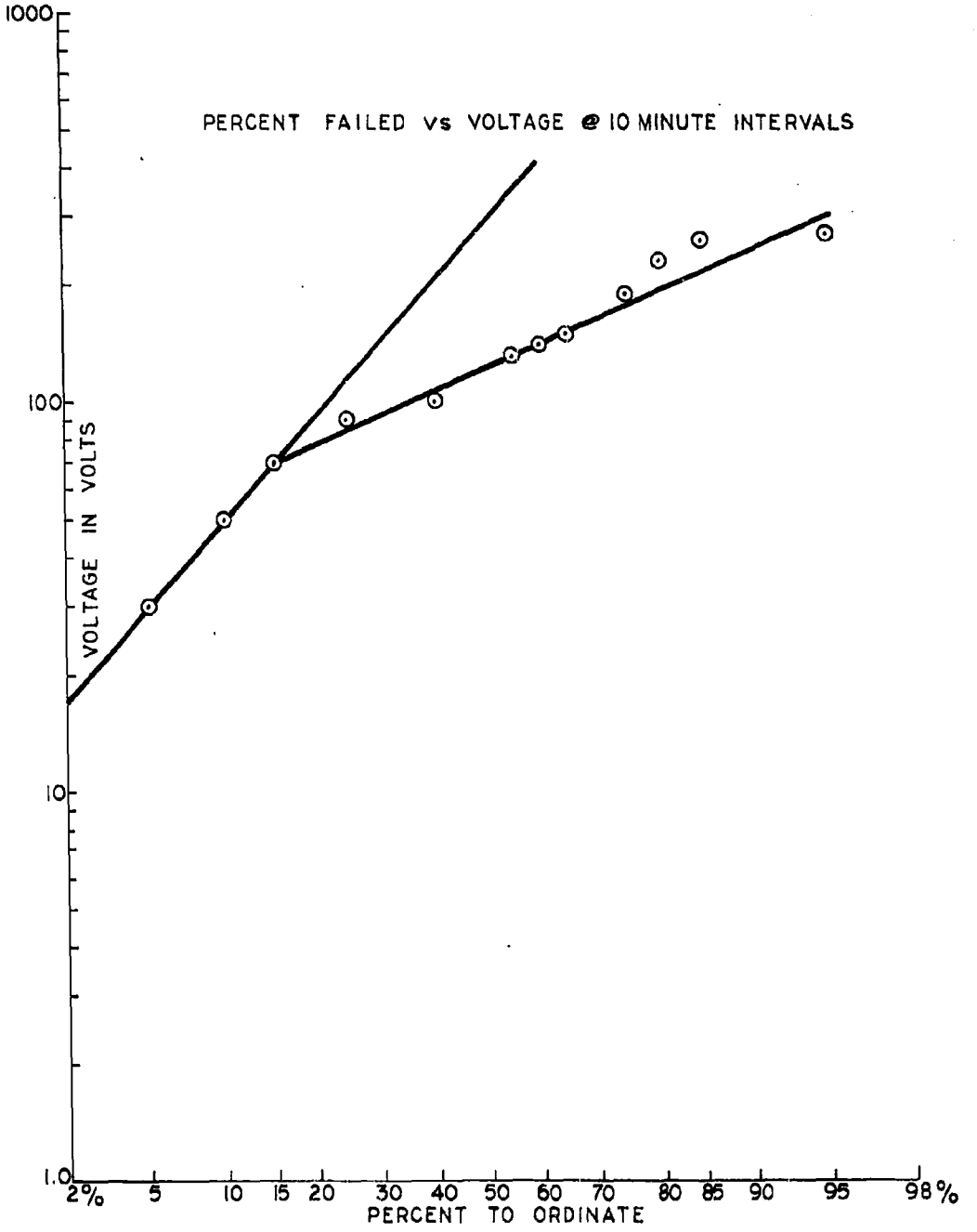


Figure 11. Capacitors Failing at Particular Voltage
10 minute Interval

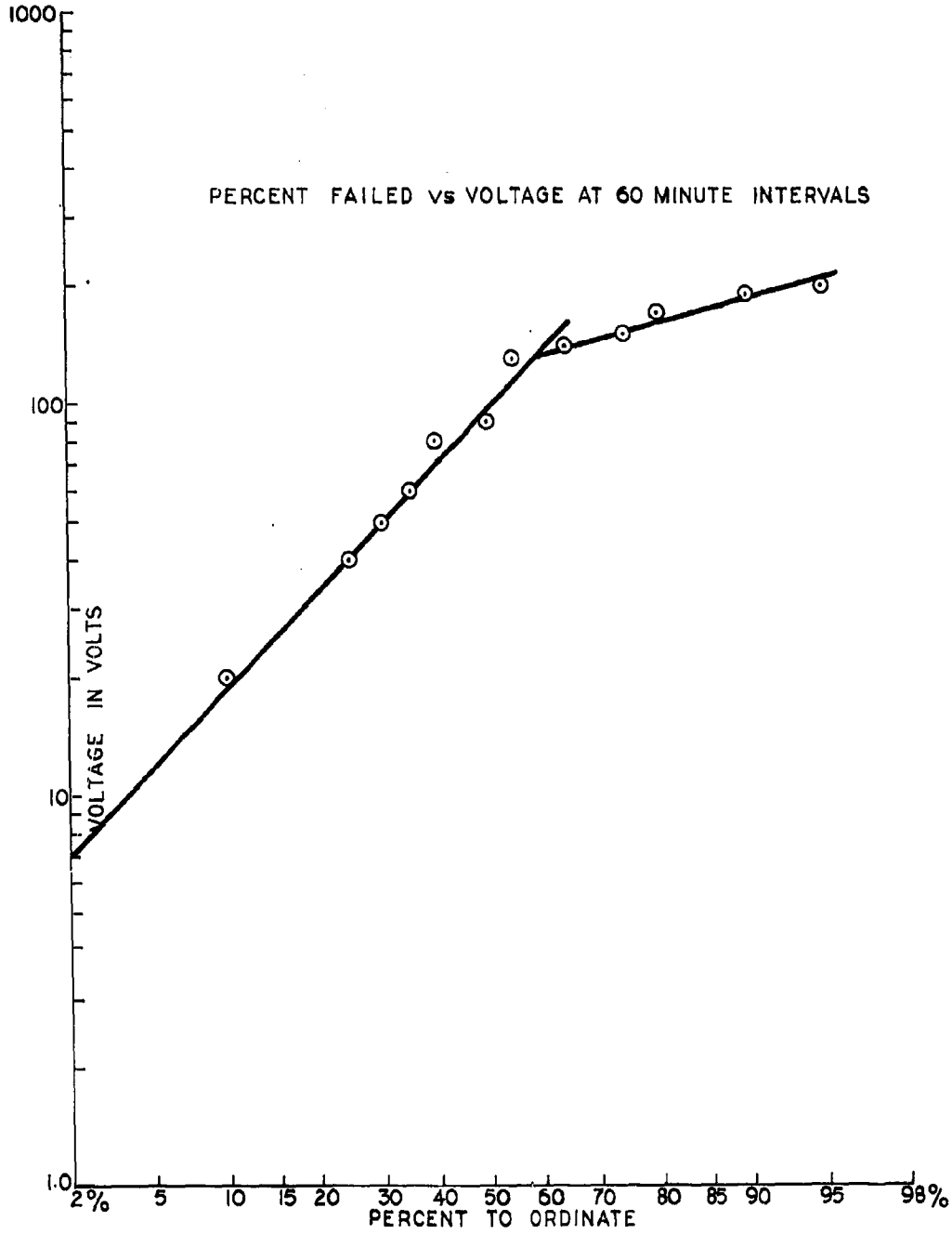


Figure 12. Capacitors Failing at Particular Voltage
60 minute Interval

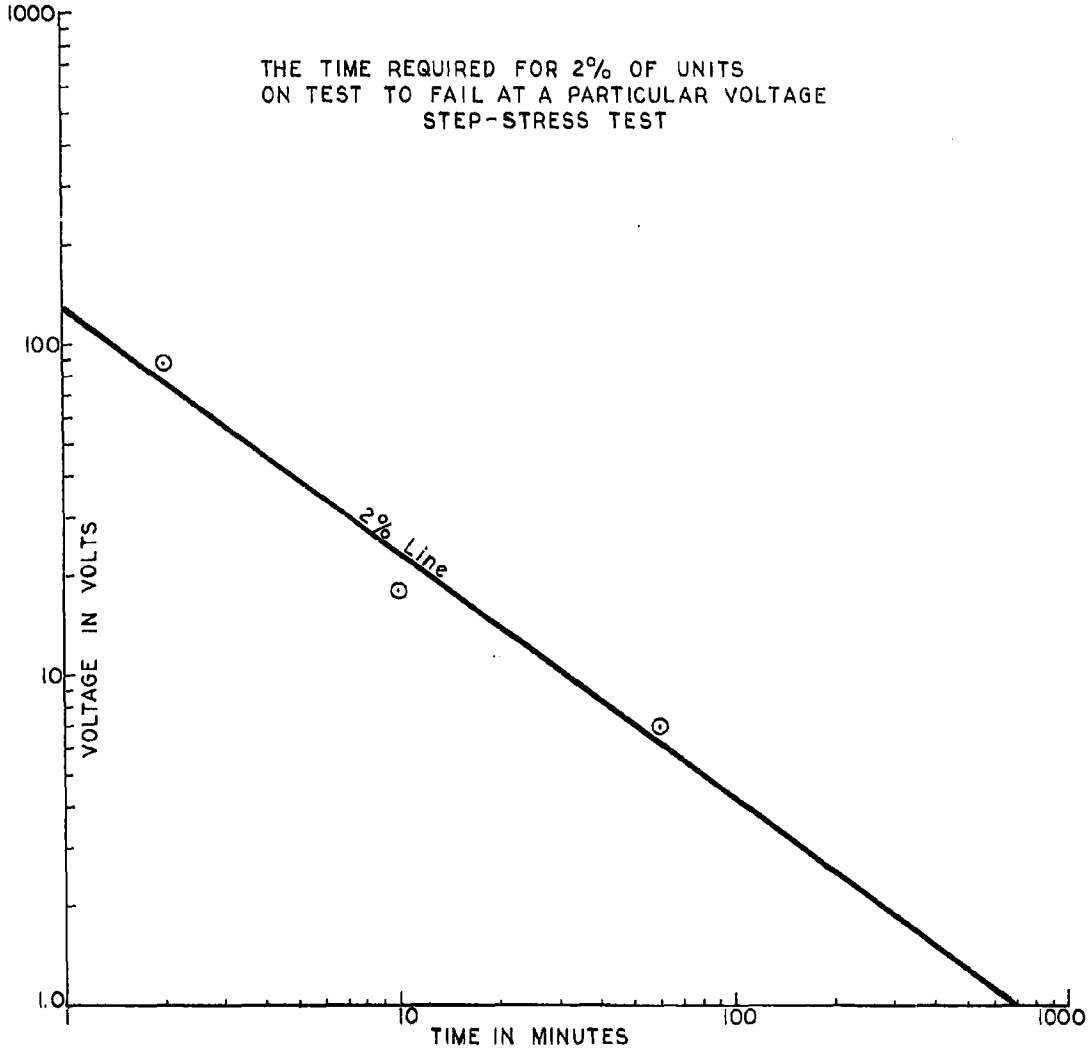


Figure 13. Voltage versus Time at 2% Failure

The formation of the silicon monoxide dielectric poses incompatibility problems with network processing.

The network bar is mounted in the header with glass frit at 450° C. Initially, the silicon monoxide was evaporated at 300° C and when raised to 450° C for mounting, very poor yields were experienced. The evaporations were then made at 400° C and the yields were slightly higher, but the majority of the capacitors were lost.

Thus far, silicon monoxide capacitors that have been made have yielded poorly, shown poor life test characteristics, and are not compatible with present processing.

C. Titanium Dioxide

Previous data on thin film capacitors using titanium dioxide as a dielectric are promising. Thus, titanium dioxide will be used for future capacitor development.

V. CIRCUIT DESIGN

Substantial circuit design was initiated in this report period, especially in the digital area. The linear circuit design has been purposely delayed because of the need for more positive results in making field-effect transistors. Heavier concentration will occur in the next report period.

A. Digital Circuit Design

In order to effectively perform logic functions when a small amount of current is available, it is necessary to use circuitry whose susceptibility to stray capacitance is small. Two circuits which should possess this trait were investigated. One was a current mode circuit as shown in Figure 14.

This type of logic has the advantage that the capacitance at certain nodes is not completely charged or discharged. Also, since the transistors are not saturated, the delay and storage times should be minimized.

The second logic type investigated was DCTL. This is shown in Figure 15.

The fall time of the circuit depends on the value of the load resistor, R_L. Therefore, the voltage of the power supply was made small so that R_L could be minimized.

Typically, the V_{BE} curves of several silicon transistors of the same type are shown in Figure 16 for 25° C. The variation of $V_{CE\ (sat)}$ and V_{BE} with temperature is shown in Figures 17 and 18. The normal operating points of these logic circuits at conditions that are not restricted by minimum power consumption are indicated on Figure 19. The $V_{CE\ (sat)}$ of an ON transistor will feed into the base of the transistors coupled to this collector and will determine if these transistors are held OFF. When the ON transistor is turned OFF, the V_{BE} voltage that exists at the collector of the

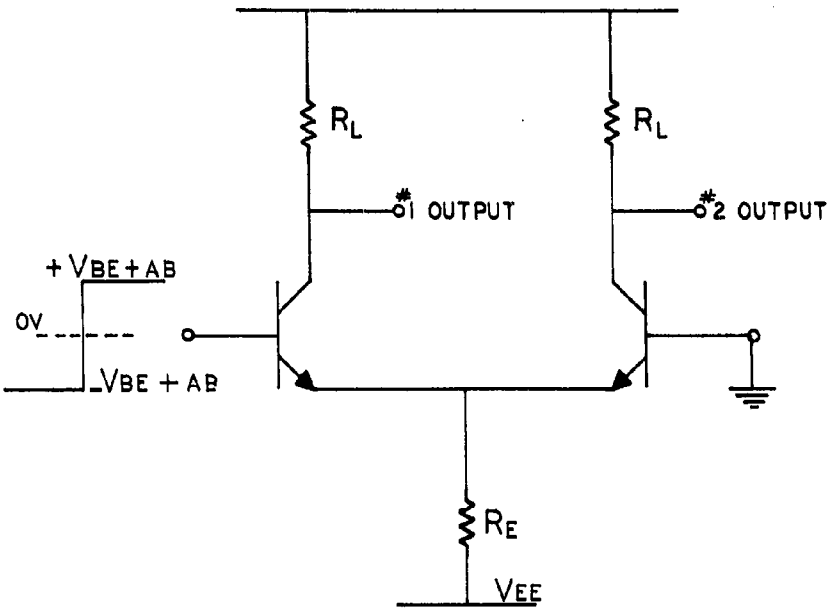


Figure 14. Current-Mode Logic Circuit

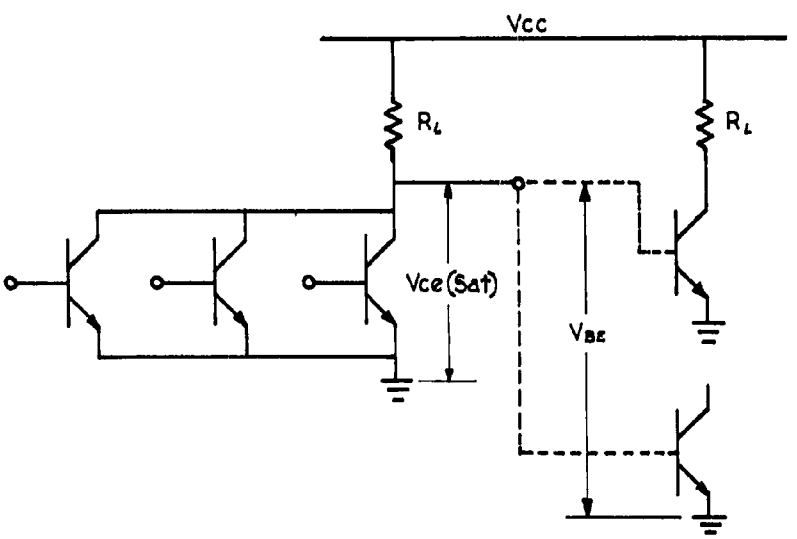


Figure 15. DCTL Logic Circuit

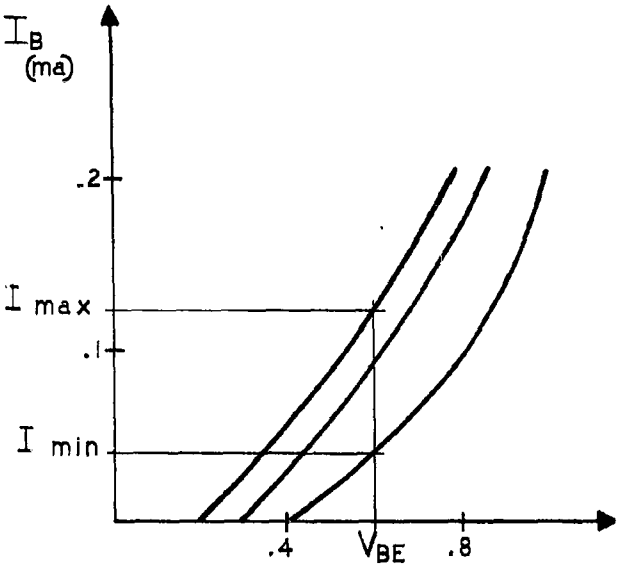


Figure 16. V_{BE} Versus I_B Silicon Transistor

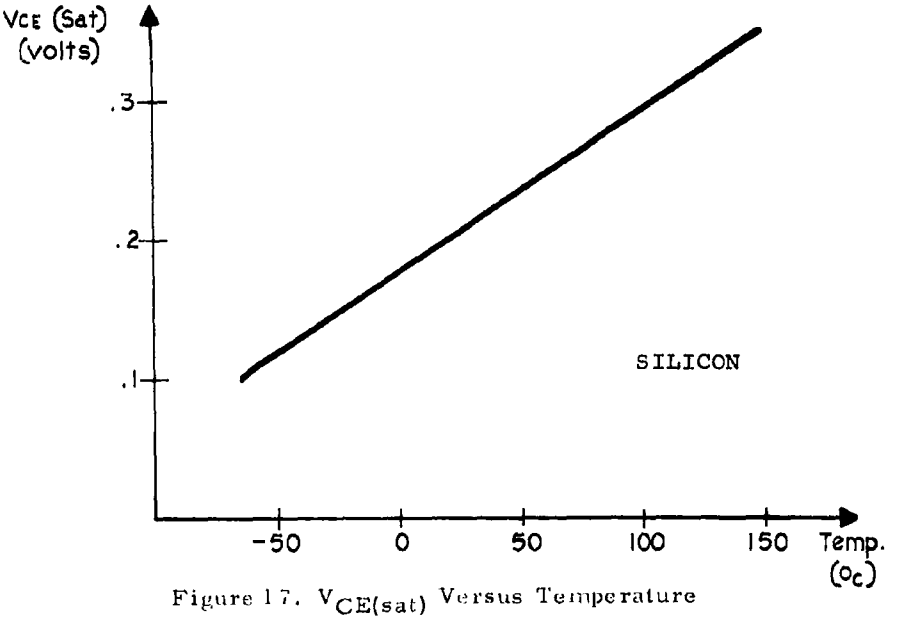


Figure 17. $V_{CE(sat)}$ Versus Temperature

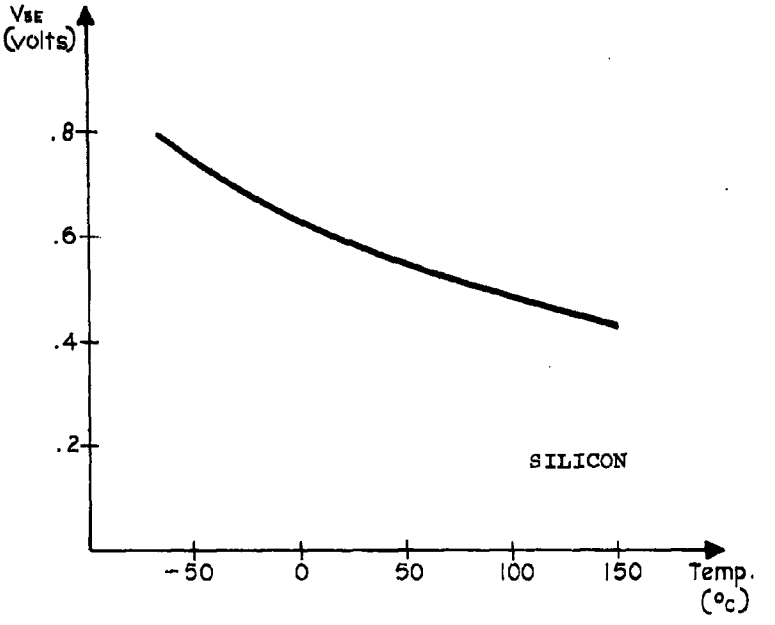


Figure 18. V_{BE} Versus Temperature

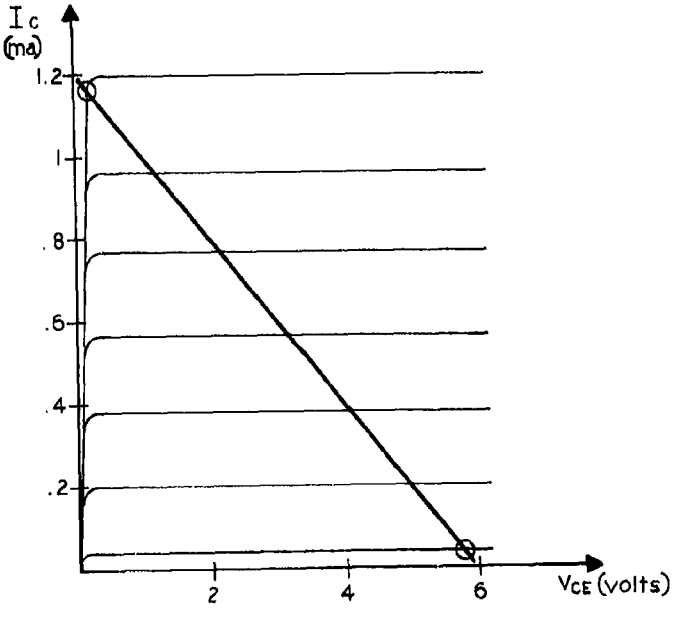


Figure 19. Operating Points of Saturated Transistor

OFF transistor and at the bases of the transistors coupled to this collector will be determined by the input impedance of each coupled transistor. Since the same V_{BE} exists at each transistor, the current into the base must be the variable. A transistor with "low" input impedance will draw more current than one with "high" input impedance. This is shown in Figure 16. This increase of current into a low impedance transistor is called current hogging. Resistors are added in the bases of each transistor to reduce the current hogging by one transistor.

When this circuit configuration is further restricted to operate at very low power, the applied voltage is reduced in value and the collector resistors are made large. This places even further severe requirements on the transistors because less total current is available and smaller variations in input impedance must be obtained to keep one transistor from hogging all the current. In addition, leakage current at high temperature is a problem. Some indication of leakage current with $V_{CE(sat)}$ is shown in Figure 20.

A circuit used for investigation in Figure 14 had V_{CC} equal to 1 volt and R_L = 40 K. Tests on this circuit with fan-out = 1 and 3 indicate that the circuitry will work successfully with V_{CC} = 1 volt.

The speed of the circuits is limited by junction capacitance, especially of the transistor. However, measurement techniques used may

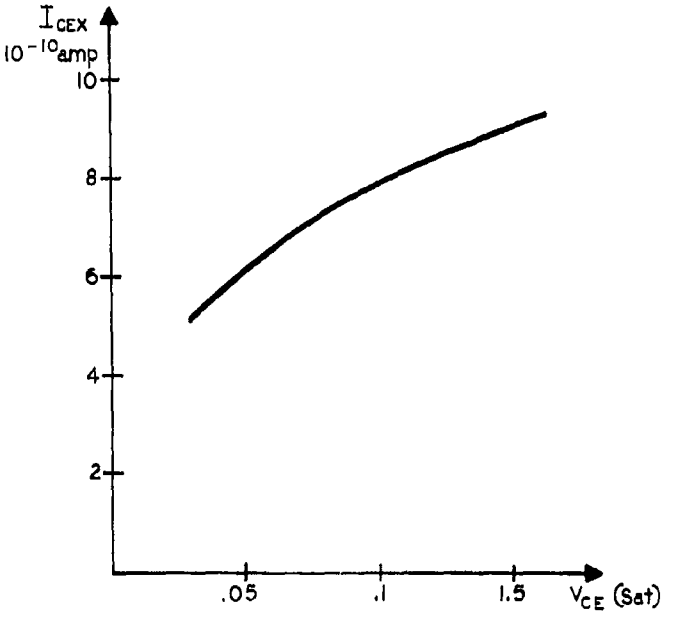


Figure 20. Leakage Current Versus $V_{CE(sat)}$

contribute significantly to increased times. For example, using a Tektronix 661 scope and probe with an input capacitance of 1.5 pf, the following switching times were obtained:

Current Mode

$t_{on} = 0.7\ \mu sec$

$t_{off} = 1.25\ \mu sec$

DCTL

$t_{on} = 1.25\ \mu sec$

$t_{off} = 0.6\ \mu sec$

Consider the t_{off} of the DCTL circuit. (A turnoff waveform is a good RC charging network.)

$$E_{RL} = E_o (1 - e^{-t/RC})$$

Let $E = 0.9\ E_o$

$$0.9 = 1 - e^{-t_1/RC}$$

$$\frac{1}{e^{-t_1/RC}} = 0.1$$

$$e^{t_1/RC} = 10$$

$$\frac{t_1}{RC} = \log_e 10$$

$$t_1 = 2.3\ RC$$

Substituting in the measured values

$$C = 6.7\ pf$$

Thus, the effect of the probe capacitance can be seen:

$$\frac{C_{probe}}{C_{total}} = \frac{1.5}{6.7} \cong 22\%$$

This illustrates the close attention that must be devoted to test circuits. Measuring techniques and instrumentation must be carefully considered.

The capacitance contributed by the junctions of the structures under development can be caluclated from a Bell Telephone Laboratories paper by H. Lawrence and R. M. Warner, Jr.*

*H. Lawrence, R. M. Warner, Jr., "Diffused Junction Depletion Layer Calculations," Bell System Technical Journal.

Table I shows calculated values of three transistor structures presently being diffused. Number 1 is a transistor from the present low-power digital networks in production at Texas Instruments. Number 2 is a transistor which is shown in Figure 21. Number 3 is a transistor of the same physical dimensions as Number 2 but with a very low concentration collector. Only the predicted capacitance values are shown for Number 3 because the transistors are now being fabricated. The measured values will be filled in for these units as soon as fabrication is complete.

Table I

Capacitance in Pf/mil^2 for Diffused Transistors

	Calculated			Measured		
Transistor	Collector to Substrate	Collector to Base	Base to Emitter	Collector to Substrate	Collector to Base	Base to Emitter
1	0.042	0.16		0.045	0.143	0.4
2	0.044	0.11	0.26	0.11	0.286	0.83
3	0.035	0.052	0.20			

Table II extends the capacitance per square mil to the total capacitance by multiplying by the area of the junctions of the transistor structures. Again, the measured values of the low collector concentration transistor, number 3, will be reported as soon as measured. Note in particular transistor number 4 which is a proposed new structure to be used in the layout for the digital circuits. The areas can be compared to the geometry shown in Figure 21, which is the size for number 2 and 3. The areas have been reduced to approximately 30 percent of the areas of numbers 2 and 3. The geometry of number 4 begins to press the photographic limits for production processes. This, of course, is a limit which it is felt should not be exceeded at this time.

Table II

Total Capacitance for Diffused Transistors

	Junction Area (mil^2)			Total Capacitance pf		
Transistor	Collector to Substrate	Collector to Base	Base to Emitter	Collector to Substrate	Collector to Base	Base to Emitter
1	155	70	25	7	10	10
2	30	10.5	3	3.3	3	2.5
3	30	10.5	3			
4	10.6	3.25	1	*1.0	*0.5	*0.5

*Predicted

The differences in measured and total capacitance are partially due to edge effects around the periphery of the junction.

For the DCTL logic gate of Figure 15, Figure 22 A is a common collector structure of three transistors with the areas shown in Table II under number 4 transistor. The total capacitance of three times collector-to-base plus three times base-to-emitter capacitance equals 3 pf. With this capacitance, the t_{OFF} times would be 0.275 microseconds using a 40K load resistor in the circuit of Figure 15 and considering that the three input bases go to ground through a low impedance. The t_{OFF} specification of 0.5 microseconds leaves about 2 pf for other capacitance present. Figure 22 B has a little larger transistor.

B. Linear Circuits

Initial linear circuit design was carried on with field-effect transistors. Some of the important considerations for these designs are as follows:

The short circuit input capacitance of the field-effect transistor should be 8 pf and have I_{DO} = 10 to 30 microamperes. Geometries of this type are feasible. Circuit work will continue to be able to apply the devices.

Because the induced-channel field-effect transistor did not prove a success, new investigations will begin using standard high gain at low collector current transistors to re-examine this area for a possible circuit solution.

VI. CONCLUSIONS

Even though the induced-channel field-effect transistor has excellent characteristics, the instability of the characteristics with temperature using the present process prevent use of this device at this time. Therefore, more effort will be placed on diffused field-effect transistor development.

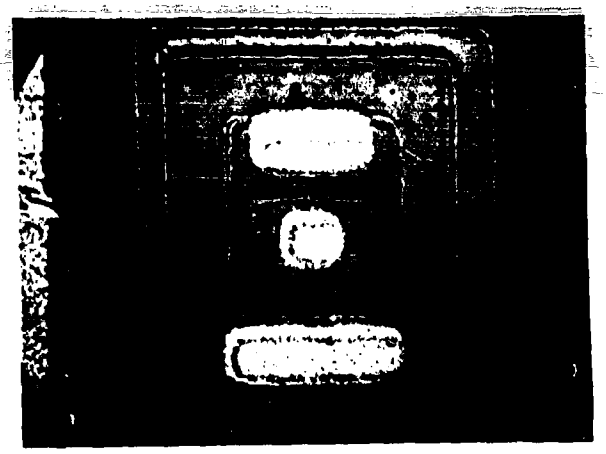
Lead glass and silicon monoxide capacitors using present process failed on life test. Lead glass dielectric shifts are due to same effect as noted for induced channel field-effect transistor. Therefore, this device will be dropped. Silicon monoxide will be investigated further.

Aluminum-silicon film resistors are being dropped because process is difficult to control.

Tantalum molybdenum resistors with 55 ppm/°C and resistivity from 1 K to 1 megohm per square have been fabricated.

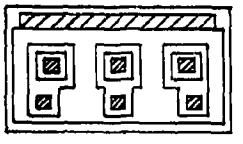
Junction capacitance will be very important to the performance of circuits, both digital and linear. However, transistor structures can be made to satisfy the performance, both in digital and linear circuits.

In linear circuits, two approaches will be followed (since the induced-channel field-effect transistor cannot be used) -- the diffused field-effect transistor circuit and a standard bipolar transistor circuit.



Collector	5 mils x 6 mils = 30 $mils^2$
Base	3 mils x 3.5 mils = 10.5 $mils^2$
Emitter	1.5 mils x 2 mils = 3 $mils^2$

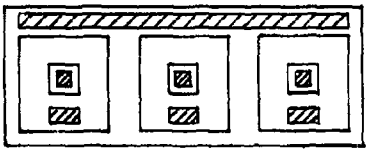
Figure 21. Small Geometry Transistor



EMITTER: 1 X 1 MIL

BASE AREA: 3.25 MIL^2

COLLECTOR: 4.25 X 7.50



EMITTER: 1 X 1 MIL

BASE AREA: 3 X 3.25

COLLECTOR: 4.75 X 12

Figure 22. Common Collector Transistor Structures

VII. PROGRAM FOR NEXT INTERVAL

Continue diffused field-effect transistor development for linear circuit application.

Continue Tantalum-Molybdenum resistor development.

Continue capacitor development.

Continue development of small geometry, low current bipolar transistors making special structures as required.

Finalize layouts for digital circuit and process material.

Finalize layouts for linear circuit and process material.

APPENDIX
KEY TECHNICAL PERSONNEL

APPENDIX

KEY TECHNICAL PERSONNEL

A. MAN HOURS

Antle, G. M.	35.0
Fottler, S. A.	185.0
Fowler, M.	147.5
Glasscock, H. W.	310.0
Harris, R.	91.0
Lathrop, J. W.	10.0
Luecke, G.	54.0
Shuey, E. H.	379.5

B. PERSONNEL RESUMES

ANTLE, GLEN M. — Associate Engineer, Integrated Circuits Group

Mr. Antle joined Texas Instruments in February 1959 as a co-op student. He spent three eight-week co-op periods in the Diode and Rectifier Department and one period in the Semiconductor Networks Department. In October 1960 he started to work in the Networks Department full time as an electronics technician. He worked in this capacity until February 1962 at which time he returned to Southern Methodist University to continue work on his degree plan in electrical engineering. Mr. Antle returned to Texas Instruments Incorporated in June 1962. In July 1962 he was promoted to the position of associate engineer. He is now attending Southern Methodist University part-time and needs two semester hours for his B.S. in Electrical Engineering.

FOTTLER, S. A. — Engineer, Slice Process Development, Integrated Circuits Group

Mr. Fottler joined the Semiconductor Networks Department in May 1960. He has worked in thin films development on capacitors and in development and mechanization work on photo resist processes. Mr. Fottler is presently directing development work on thin films for resistors, capacitors and interconnections. Prior to joining Texas Instruments Incorporated Mr. Fottler worked six years for General Motors Corporation in physics research and development.

FOWLER, M. A. — Engineer, Process Development Branch, Semiconductor Networks Department

B. S. in Physics, Texas Technological College

Miss Fowler is presently engaged in process development of both P- and N-type diffusions as well as being on a special task force for technical advisement in the Networks manufacturing area. She was previously engaged in developing processes for various triple- and quadruple-diffused units.

GLASSCOCK, H. W. — Associate Engineer
Integrated Circuits Engineering

B. S. in Electrical Engineering, University of Arkansas
Member of Tau Beta Pi and Eta Kappa Nu

Mr. Glasscock joined Texas Instruments, Apparatus Division, June 1959, and until May of 1960 was engaged in the study of underwater sound propagation and submarine detection. From May 1960 to September 1960 he was engaged in circuit development in the Magnetics Section at which time he transferred to the Semiconductor-Components Division. From September 1960 to September 1962 he was engaged in the design of test equipment and device evaluation. He is presently engaged in device diffusion studies on semiconductor networks.

HARRIS, R. E. — Engineer, Slice Process Development
Integrated Circuits Group

B. S. in Physics, Purdue University
Member of American Physical Society

Mr. Harris joined the Semiconductor Networks Department in June 1960. He has worked with the development and evaluation of silicon diffusion techniques and the analytic treatment of diffused layer electrical characteristics. His recent work has been in the field of thermally grown glass films for network capacitors and surface field-effect devices.

LATHROP, JAY W. — Manager, Networks Technology
Integrated Circuits Group

Ph. D. in Physics, Massachusetts Institute of Technology
M. S. in Physics, Massachusetts Institute of Technology
B. S. in Physics, Massachusetts Institute of Technology
Member of American Physical Society, Sigma Xi, and Electrochemical Society

A member of the technical staff since 1958, Dr. Lathrop is presently responsible for direction of chemists and physicists engaged in the development of new and improved process techniques for silicon semiconductor networks. He is also responsible for the fabrication of engineering samples of new designs and the control of manufacturing processes. Previsouly, he was a senior engineer in the Device Electronics Branch of the Research and Engineering Department where he was responsible for the development of photo engraving and oxide masking techniques applied to diffused silicon transistors and for device structure investigations. From 1953 to 1958 Dr. Lathrop was employed by the Diamond Ordnance Fuze Laboratories, Washington, D. C., where he conducted research and development work on semiconductor devices applicable to 2D techniques. He was a member of a five-man team awarded the Department of Army Civilian Meritorious Award in 1959. Dr. Lathrop is author of numerous papers and articles for technical publications.

LUECKE, GERALD — Manager, Design Branch
Integrated Circuits Group

B. S. in Electrical Engineering, University of Iowa
M. S. in Electrical Engineering, Northwestern University

Mr. Luecke joined Texas Instruments Incorporated in 1957. His major responsibility at that time was the application of transistor switches. He later served as group leader in the applications section on switching circuits, and in semiconductor networks. He was then appointed Manager of Computer and Applications Branch of the Marketing Department. Before coming to Texas Instruments Incorporated, Mr. Luecke was employed by the Victor Adding Machine Company, Chicago, Illinois. While in their employ, he worked as a circuit design engineer on telemetry equipment, flight test data accumulation and reduction equipment, and transistorized digital equipment.

SHUEY, EDWIN H. — Engineer, Design Branch
Integrated Circuits Group

B. S. in Electrical Engineering, Carnegie Institute of Technology

Mr. Shuey joined Texas Instruments in June 1962 after graduation. He has worked in the digital section of the Integrated Circuits Group and has done design work on integrated digital circuits.

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Unclassified Report

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1. Transistors—Design
2. Transistors—Development
3. Resistors—Design
4. Resistors—Development
5. Capacitors—Design
6. Capacitors—Development

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II. Luecke, Gerald
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Diffused field-effect transistors were fabricated but the I_{DO} was not low enough. Units did not have the back gates isolated.

Circuit design progressed in the digital area to the point of applying components to a specific layout.

Linear circuit design was begun during this quarter.

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